CLAIMS

1. A circuit testing apparatus comprising:

a controller for controlling signals being transferred between a circuit under test and the circuit testing apparatus; and

a driver circuit for generating signals to be applied to the circuit under test, the driver circuit includes a high speed slave chain and a DC control loop chain coupled to the circuit under test, the high speed slave chain receives a differential voltage logic pulse train and converts said logic pulse train into an high speed current steering for producing said drive signal to be applied to the circuit under test, the DC control loop chain provides feedback paths for DC regulation of inputs of said high speed slave chain.

2. The circuit testing apparatus of claim 1, wherein the driver is a class A driver.

3. The circuit testing apparatus of claim 1, wherein the driver circuit is coupled to a pin on the circuit under test.

4. The circuit testing apparatus of claim 1, further comprising a receiver circuit for receiving output signals from the circuit under test.

5. The circuit testing apparatus of claim 4, wherein the receiver circuit is coupled to a pin on the circuit under test.

6. The circuit testing apparatus of claim 4, wherein the receiver circuit and the driver circuit are coupled together to a pin on the circuit under test.

7. The circuit testing apparatus of claim 1, wherein the high speed slave chain further includes an input clamp stage for receiving said differential logic pulse train and converting said differential logic pulse train into fixed amplitude complimentary output voltages.

8. The circuit testing apparatus of claim 1, wherein the DC control loop chain further includes an input clamp stage for receiving fixed differential logic signals and converting said fixed differential logic pulse train into fixed amplitude complimentary output voltages.

9. The circuit testing apparatus of claim 8, wherein the high speed slave chain and DC control loop chain further include a current controlled gain stage for receiving fixed amplitude complimentary output voltages of the input clamp stage and employing a controlled cascode translinear multiplier cell configuration to provide a wide bandwidth with high DC precision and low distortion means of controlling the amplitude.

10. The circuit testing apparatus of claim 9, wherein the high speed slave chain and DC control loop further includes an output stage that is a standard cascaded differential linear amplifier.

11. The circuit testing apparatus of claim 10, wherein the output stage of the high speed slave chain whose output currents drive an output resistor of the said driver.

12. The circuit testing apparatus of claim 10, wherein the output stage of DC control loop chain provides feedback currents to DC control loop chain

13. The circuit testing apparatus of claim 1, wherein the high speed slave chain and DC control loop chain further comprises an output stage that includes a differential-input pair of transistors which receive a differential voltage input signal to drive the their respective output stage circuits.

14. The circuit testing apparatus of claim 13, wherein the output stage further includes a pair of transistors that receive a single-ended voltage input.

15. The circuit testing apparatus of claim 14, the output stage further includes a resistance coupled between the transistors, the differential voltage input signal controlling an amount of current through the resistance to control a current level in each of the transistors to generate the drive signal applied to the circuit under test.

16. The circuit testing apparatus of claim 14, the output stage further includes a pair of current sources coupled to the transistors, each of the current sources driving a respective current through a respective one of the pair of transistors.

17. The circuit testing apparatus of claim 16, the output stage further includes a resistance coupled between the transistors, the differential voltage input signal controlling an amount of current through the resistance to control a current level in each of the transistors to generate the drive signal applied to the circuit under test.

18. The circuit testing apparatus of claim 9, wherein the transistors are bipolar junction transistors.

19. A circuit testing apparatus comprising:

controlling means for controlling signals being transferred between a circuit under test and the circuit testing apparatus; and

driving means for generating signals to be applied to the circuit under test, the driver circuit includes a high speed slave chain and a DC control loop chain coupled to the circuit under test, the high speed chain circuit receives a differential voltage logic pulse train and converts said logic pulse train into an high speed current steering for producing said drive signal to be applied to the circuit under test, the DC control loop chain provides feedback paths for DC regulation of inputs of said high speed slave chain.

20. The circuit testing apparatus of claim 19, wherein the driver is a class A driver.

21. The circuit testing apparatus of claim 19, wherein the driver circuit is coupled to a pin on the circuit under test.

22. The circuit testing apparatus of claim 19, further comprising a receiver circuit for receiving output signals from the circuit under test.

23. The circuit testing apparatus of claim 22, wherein the receiver circuit is coupled to a pin on the circuit under test.

24. The circuit testing apparatus of claim 22, wherein the receiver circuit and the driver circuit are coupled together to a pin on the circuit under test.

25. The circuit testing apparatus of claim19, wherein the high speed slave chain further includes an input clamp stage for receiving said differential logic pulse train and converting said differential logic pulse train into fixed amplitude complimentary output voltages.

26. The circuit testing apparatus of claim 19, wherein the DC control loop chain further includes an input clamp stage for receiving fixed differential logic signals and converting said fixed differential logic pulse train into fixed amplitude complimentary output voltages.

27. The circuit testing apparatus of claim 26, wherein the high speed slave chain and DC control loop chain further include a current controlled gain stage for receiving fixed amplitude complimentary output voltages of the input clamp stage and employing a controlled cascode translinear multiplier cell configuration to provide a wide bandwidth with high DC precision and low distortion means of controlling the amplitude.

28. The circuit testing apparatus of claim 27, wherein the high speed slave chain and DC control loop further includes an output stage that is a standard cascoded differential linear amplifier.

29. The circuit testing apparatus of claim 28, wherein the output stage of the high speed slave chain whose output currents drive an output resistor of the said driver.

30. The circuit testing apparatus of claim 29, wherein the output stage of DC control loop chain provides feedback currents to DC control loop chain

31. The circuit testing apparatus of claim 19, wherein the high speed slave chain and DC control loop chain further comprise an output stage that includes a differential-input pair of transistors which receive a differential voltage input signal to drive the their respective output stage circuits.

32. The circuit testing apparatus of claim 31, wherein the output stage further includes a pair of transistors that receive a single-ended voltage input.

33. The circuit testing apparatus of claim 32, the output stage further includes a resistance coupled between the transistors, the differential voltage input signal controlling an amount of current through the resistance to control a current level in each of the transistors to generate the drive signal applied to the circuit under test.

34. The circuit testing apparatus of claim 33, the output stage further includes a pair of current sources coupled to the transistors, each of the current sources driving a respective current through a respective one of the pair of transistors.

35. The circuit testing apparatus of claim 34, the output stage further includes a resistance coupled between the transistors, the differential voltage input signal

controlling an amount of current through the resistance to control a current level in each of the transistors to generate the drive signal applied to the circuit under test.

36. The circuit testing apparatus of claim 31, wherein the transistors are bipolar junction transistors.

37. A method of testing a circuit, comprising:

providing a controller for controlling signals being transferred to and from the circuit under test;

providing a driver circuit coupled to the circuit under test;

receiving a differential voltage logic pulse train; and

converting said logic pulse train into a high speed current steering for producing said drive signal to be applied to the circuit under test.

38. The circuit testing apparatus of claim 37, wherein the driver circuit is a class A driver.

39. The circuit testing apparatus of claim 37, wherein the driver circuit is coupled to a pin on the circuit under test.

40. The circuit testing apparatus of claim 37, further providing a receiver circuit for receiving output signals from the circuit under test.

41. The circuit testing apparatus of claim 40, wherein the receiver circuit is coupled to a pin on the circuit under test.

42. The circuit testing apparatus of claim 41, wherein the receiver circuit and the driver circuit are coupled together to a pin on the circuit under test.

43. The circuit testing apparatus of claim 38, wherein receiving said differential logic pulse train further includes converting said differential logic pulse train into fixed amplitude complimentary output voltages.

44. The circuit testing apparatus of claim 38, further comprising receiving fixed differential logic signals and converting said fixed differential logic pulse train into fixed amplitude complimentary output voltages.

45. The circuit testing apparatus of claim 44, further comprising receiving fixed amplitude complimentary output voltages and employing a controlled cascode translinear multiplier cell configuration to provide a wide bandwidth with high DC precision and low distortion means of controlling the amplitude.

46. The circuit testing apparatus of claim 44, wherein the driver circuit further includes a standard cascoded differential linear amplifier.